AMENDMENTS TO CLAIMS

• Please amend pending claims 1, 6, 11, and 16 as indicated below. A complete listing of all claims and their status in the application are as follows:

1. (currently amended) A method for facilitating semiconductor wafer lot disposition, comprising:

providing detailed descriptive information of the semiconductor wafer layout;

locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot to generate data concerning at least one defect in the semiconductor wafer at an intermediate processing stage;

generating at least one layer model from the information and data to disclose the effects of the at least one defect upon at least one later layer of the semiconductor wafer; and

utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot, including whether to proceed with further processing of the wafer production lot.

2. (previously presented) The method of claim 1 wherein generating the at least one layer model further comprises disclosing the components that will be located above the at least one defect in the semiconductor wafers.

3. (previously presented) The method of claim 1 wherein utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises treating the data concerning the at least one defect as a new layer of information.

4. (previously presented) The method of claim 1 wherein utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises determining whether the at least one defect would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between layers.

5. (previously presented) The method of claim 1 wherein providing detailed descriptive information of the semiconductor wafer layout further comprises providing an

electronic description of the semiconductor wafer layout for substantially every layer in the semiconductor wafers' fabrication process.

6. (currently amended) A method for facilitating semiconductor wafer lot disposition, comprising:

providing detailed descriptive information of the semiconductor wafer layout;

locating and defining current defects in partially completed dies of semiconductor wafers in a wafer production lot to generate and extract data concerning defects in the semiconductor wafers at an intermediate processing stage;

generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the semiconductor wafers' fabrication process; and

utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot, including whether to proceed with further processing of the wafer production lot.

7. (previously presented) The method of claim 6 wherein generating the at least one layer model further comprises disclosing the components that will be located above the defects in the semiconductor wafers.

8. (previously presented) The method of claim 6 wherein utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises treating the data concerning the future defects as a new layer of information.

9. (previously presented) The method of claim 6 wherein utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises determining whether the current defects would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between various layers.

10. (previously presented) The method of claim 6 wherein providing detailed descriptive information of the semiconductor wafer layout further comprises providing an electronic description of the semiconductor wafer layout for substantially every layer in the semiconductor wafers' fabrication process.

11. (currently amended) A system for facilitating semiconductor wafer lot disposition, comprising:

means for providing detailed descriptive information of the semiconductor wafer layout;

means for locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot to generate data concerning at least one defect in the semiconductor wafer at an intermediate processing stage;

means for generating at least one layer model from the information and data to disclose the effects of the at least one defect upon at least one later layer of the semiconductor wafer; and

means for utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot, including whether to proceed with further processing of the wafer production lot.

12. (previously presented) The system of claim 11 wherein the means for generating the at least one layer model further comprises means for disclosing the components that will be located above the at least one defect in the semiconductor wafers.

13. (previously presented) The system of claim 11 wherein the means for utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises means for treating the data concerning the at least one defect as a new layer of information.

14. (previously presented) The system of claim 11 wherein the means for utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises means for determining whether the at least one defect would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between layers.

15. (previously presented) The system of claim 11 wherein the means for providing detailed descriptive information of the semiconductor wafer layout further comprises means for providing an electronic description of the semiconductor wafer layout for substantially every layer in the semiconductor wafers' fabrication process.

16. (currently amended) A system for facilitating semiconductor wafer lot disposition, comprising:

means for providing detailed descriptive information of the semiconductor wafer layout;

means for locating and defining current defects in partially completed dies of semiconductor wafers in a wafer production lot to generate and extract data concerning defects in the semiconductor wafers at an intermediate processing stage;

means for generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the semiconductor wafers' fabrication process; and

means for utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot, including whether to proceed with further processing of the wafer production lot.

17. (previously presented) The system of claim 16 wherein the means for generating at least one layer model further comprises means for disclosing the components that will be located above the current defects in the semiconductor wafers.

18. (previously presented) The system of claim 16 wherein the means for utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises means for treating the data concerning the defects as a new layer of information.

19. (previously presented) The system of claim 16 wherein the means for utilizing the at least one layer model to determine the subsequent disposition of the wafer production lot further comprises means for determining whether the current defects would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between various layers.

20. (previously presented) The system of claim 16 wherein the means for providing detailed descriptive information of the semiconductor wafer layout further comprises means for providing an electronic description of the semiconductor wafer layout for substantially every layer in the semiconductor wafers' fabrication process.